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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,225	09/12/2003	Huy Nguyen	60809-0132-US	6839

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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,225	NGUYEN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12-10-04;05-03-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Claim 1 is indefinite because it is not clear which drawing the claim reads on. Assume that claim 1 reads on figure 2C of the present application. Buffer (206) receives a system clock signal. There is no circuit seen in figure 2C that detects the duty cycle of a data signal as recited on line 3 of the claim. Circuit (242) only compares Data Signal (226) with an output from circuit (240) thus circuit (226) is not the circuit that detects the duty cycle of the data signal (226). The recitation "comparing the detected duty cycle with a predetermined duty cycle" on line 4 is indefinite because it is not clear as to "the detected duty cycle" is the detected duty cycle of the data signal or the detected duty cycle of the system clock. The recitation "detecting a duty cycle of a data signal" on line 3 is indefinite because it is misdescriptive. Figure 2C does not show any circuit that detects a duty cycle of a data signal. Figure 2D could be a circuit that detects a duty cycle of a data signal but it is not clear how this circuit can be implemented into the circuit of figure 2C. Moreover, figure 2D is only a level detector that detects a high/low level of the clock/data signal then this high/low level is compared with a reference voltage. The circuit of figure 2D is not seen to detect the duty cycle of a data signal that is defined as an amount of time the data is high (low) with respect to the whole cycle of data signal. The same rationale is applied to claims 2,6, 8, 9, 11, 12, 13, 14, 16, 18, 21, 22, 24, 27, 28, 29, 30, 31, 32, 33, 34, 35-39 and 42.

Regarding claim 2, the recitation "the step of detecting the duty cycle of a data signal comprises the detecting a first duty cycle of a first data signal from a first device, and detecting a second duty cycle of a second data signal from a second device" on lines 1-4 is indefinite because it is confusing. Figure 2C of the present application shows that there is no circuit that detects "duty cycle of a data signal" seen. Assume that circuit (226) detects the

duty cycle of a data signal. It is not clear how this circuit can detects multiple data signals from multiple devices as recited. The recitation "the step of comparing the detected duty cycle" on line 5 is indefinite because it is not clear as to this "detected duty cycle" is the detected duty cycle of the data signal or the detected duty of the system clock.

Regarding claim 6, the recitation " the predetermined duty cycle" on line 3-4 is indefinite because it is not clear as to this " the predetermined duty cycle" is the same or different than "a predetermined duty cycle" on line 4 of claim 1. The Applicant is requested to show what drawing the circuit of claims 1-20 reads on. The Applicant is requested to point out which drawing the circuit of claims 1-20 reads on.

Claim 21 is indefinite because it is not clear what drawing(s) the circuit of claim 21 is read on. It is not clear what are the: "clock receiver", " a data signal duty cycle detector" and "a receiver clock generator" in the drawings. As understood by the examiner, the clock receiver may be shown in figure 2A or figure 2C, "a data signal duty cycle detector" may be shown in figure 2D, "a receiver clock generator" is not seen in any drawing. The Applicant is requested to point out a circuit comprising "a clock receiver", " a data signal duty cycle detector", "a receiver clock generator" and to show how connect these separate circuits to form a single circuit that is the claimed "integrated circuit". The Applicant is requested to point out which drawing the circuit of claims 21-41 reads on.

Claim 27 is indefinite because it is not clear what are the "a clock cycle detector", "a second correction circuit" in the drawing(s).

Regarding claim 42, the recitations "means for receiving a system clock signal" "means for detecting a duty cycle of a data signal" and "means for generating a receiver clock signal" are indefinite because it is not clear what are these means in the drawing(s). The Applicant is requested to point out which drawing the circuit of claim 42 reads on.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 21-26, 34, 35 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Desai (US. 6,862,296).

Regarding claims 1-4, figure 5 of Desai shows a method of adjusting a receiver clock duty cycle, comprising:

receiving a system clock signal (Recovered clock);

detecting a duty cycle of a data signal and comparing the detected duty cycle with a predetermined duty cycle (Reference Pattern) in order to determine a first difference (Match) between the detected data signal duty cycle and the predetermined duty cycle;

generating a receiver clock (Word Clock) from the system clock signal; and

adjusting a duty cycle of the receiver clock in accordance with the first difference between the detected data signal duty cycle and the predetermined duty cycle. Comparator (508) detects the duty cycle of data signal (Received Data) and compares the detected duty cycle with a predetermined duty cycle (Reference Pattern). The duty cycle of the receiver clock is adjusted by varying the value of the (Reference Pattern) signal. Figure 7 shows that the data are different.

Regarding claims 21-26, 34, 35, figure 5 of Desai shows an integrated circuit, comprising:

a clock receiver configured to receive a system clock signal (Recovered Clock) having a duty cycle;

a data signal duty cycle detector (508) configured to detect a first duty cycle of a first data signal and to generate a first difference signal representing a difference between the first duty cycle and a first predetermined duty cycle (Reference Pattern); and

a receiver clock generator (506) configured to output a receiver clock signal (Word Clock) based on the system clock signal and the first difference signal (Shift), the receiver clock generator including a first correction circuit configured to adjust a duty cycle of the receiver clock signal in accordance with the first difference signal. Depending on the various values of the data signal, the second, third difference signals and receiver clock signal are generated. The first and second predetermined duty cycles (Reference Pattern) can be

varied. The data signals can be generated from different devices located on different ICs. The predetermined duty cycle can be adjusted as required.

Regarding claim 42 figure 5 of Desai shows an integrated circuit, comprising: an integrated circuit, comprising:

means for receiving a system clock signal (506) having a duty cycle; means for detecting a duty cycle of a data signal (508) and for generating a first difference signal (Shift) representing a difference between the detected data signal duty cycle and a predetermined duty cycle; and

means for generating a receiver clock signal (506) based on the system clock signal and the first difference signal, including means (500) for adjusting a duty cycle of the receiver clock signal in accordance with the first difference signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 13, 14,18-20 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai (US. 6,862,296).

Regarding claims 5, 13, 14,18-20 and 39-41 figure 5 of Desai includes all the limitations of these claims except for different values of the duty cycles, the difference and the sources of the data signal. However, it is well known to one of ordinary skill in the art that first difference can be set to desired value and the data signals can be provided from different Ics and the first and second device can be located on different Ics can be adjusted to proper duty cycles.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen
01-25-07

TUAN T. LAM
PRIMARY EXAMINER